ARRAY

DEVELOPMENT PLAN

FOR THE IMPLEMENTATION OF:

SCALABLE COMPUTE-IN-MEMORY WITH
+80% EFFICIENCY AND THROUGHPUT GAINS
USING STANDARD CMOS TECHNOLOGY

www.arrayarchitecture.com

Given that we have proven and verified the Register-Transfer-Level design in VHDL simulation, the next 16 months are about further de-risking the technology at a physical level and creating the licensable asset (GDSII tape-out ready Stream File). Our cash burn-rate will be primarily driven by the engineering team's salaries, signing bonuses, tools, and resources. The investment is divided in two stages: The first stage lasting **6 months** requires a capital investment of **$500k USD to validate and benchmark** key parameters of the arithmetic core. The second stage, lasting **10 months** requires a capital investment of **$6.1 Million USD to prototype a Compute-In-Memory Mining Engine or AI Accelerator.** Our goal is to deliver silicon-ready files within 16 months. The verified and patented prototype architecture will be licensed to larger designers and manufacturers.

Key deliverables include real-world FPGA emulation, and GDSII pre-silicon files for a **first-of-its-kind ASIC prototype,** as well validated benchmarking through industry-grade tools and lab testing. The project is **structured around two highly skilled teams,** one for RTL to GDSII Flow and one for FPGA/testing, lead by a Senior ASIC Physical Design Engineer, and supported by dedicated workstations and infrastructure.

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Next-Generation Bitcoin Mining ASIC

Project Brief

Deliverables

- **FPGA Emulation**: Energy/Latency Benchmarks.
- **Validation:** Test Physical Circuit Board (PCB).
- Pre-Production **GDSII Stream File**.

Project Goals

- Design for **Compute-In-Memory Mining ASIC**.
- Emulate and Benchmark Against Existing Architectures.
- Patent CIM Mining ASIC.
- Publish Results Reflecting Significant **Energy Savings**, and **Minimum Latency**.

Project Objective

Prototype for First Compute-In-Memory Mining ASIC

Technology

- **FIRST IN-MEMORY MINING ASIC IN THE MARKET**
- **High-Performance (+Hashes/second)**
- **Low-Power (+Hashes/Joule)**

Project Leads

Senior Staff Engineer

Design Team. Consists of (1) Sr. ASIC Eng. and (2) Jr. RTL Engs.

Testing Team. Consists of (1) Sr. ASIC Eng. and (2) Jr. FPGA Engs.

Support Team

- **CAD Flow and Support Team**
- **Graduate Students (2-4)**
- **Core Team**
  - **Architect and General Manager**
  - **Administrative Management**
  - **Scripting and Environment Support**

16-Month Timeline

1. Team Onboarding
2. RTL Development
3. FPGA Emulation & Benchmarking
4. Prototype ASIC

Key Milestones

1. Prototype Arithmetic Core
2. Integration to ASIC Design Standards
3. Integration to ASIC Manufacturing Standards

Expected Outcomes

- **Efficient Synthesis of ASIC Design**
- **Confirm Expected Performance**
- **Tapeout Ready Prototype**

Resources

Workstations

Lab Equipment

Electronic Design Automation Software

FPGAs

$6.6 Million USD

- **Professional-Grade Verification**
- **Realistic Emulation**
- **Trusted Measurements**
- **Scalabillity**
- **No Productivity Bottlenecks**
- **Team Readiness**

16-Month Timeline

Phases

Building an FPGA prototype is paramount because it will provide the first real-world validation of the SLFA's timing, control logic, and area efficiency, informing all subsequent ASIC design decisions. We have a 16-Month Development Plan, divided into 3 phases that make distinction between 1) Validating the arithmetic core, from the more complex task of 2) building a full system around it, and then 3) taking it to Physical Design. These are three distinct challenges.

Phase I: Prototype Arithmetic Core (6 Month Mark). A Fully Functional and Verified Core arithmetic unit (a 32-bit adder/multiplier based on FAU) is emulated and completely verified for functional correctness. We will design, verify, and benchmark the FAU's "local operability", functional correctness, performance, and power characteristics in isolation, proving its fundamental advantage and further de-risking the technology. Before a single line of code is written, the team must fully understand and define the microarchitecture. How does the data flow? How are registers organized? How is memory accessed? The following months are for designing the adder architecture and local operability to prove the core IP works. The arithmetic unit (a 32-bit adder/multiplier based on our FAU) is verified for functional correctness and to provide the data needed to secure licensing deals.

i. Onboarding
ii. Implement Registers in Verilog
iii. RTL Design of CIM Adder
iv. Verify and Test
v. Emulate and Benchmark
iv. Publish Results

Phase II: Integration to ASIC Design Standards (12 Month Mark). The 12-month milestone is to integrate the arithmetic core into a complete System-on-Chip for a SHA-256 hashing pipeline. This includes integration to the surrounding infrastructure for the core: control logic, memory interfaces, data movement, and I/O to create a functional system.

i. Define RTL Layout
ii. Building surrounding infrastructure of core for control logic
ii. Synopsys UVM/VCS Verification
iii. Emulate and Benchmark

Phase III: Integration to ASIC Manufacturing Standards (16 Month Mark). The 16 month milestone is to have a complete "prototype" as an industry-grade pre-silicon GDSII files ready to be sent to a foundry for fabrication. The tapeout-ready GDSII Stream File is the complete design file asset and is incredibly valuable for licensing. Our goal is to design a novel hardware architecture, prove correctness of its functionality, characterize its performance and generate Pre-Silicon files in order to license the underlying IP. We will be delivering a validated design database ready for manufacturing and System-Level Verification Report including extensive testing showing the integrated system meets all functional and performance targets. The complete RTL to GDSII Flow consists of:

i. Synthesis
ii. Design for Testability
iii. Floor planning (Place & Route)
iv. Clock Tree Synthesis (CTS)
v. Manufacture Prep

16-Month Timeline

Phase I: Prototype Arithmetic Core | (Months 1-6)

Goals	Key Tasks	Deliverables
FPGA High-Speed Emulation of Proof-of-Concept (run arithmetic core on FPGA) Standard Cell Library Integration: Characterize the performance of our SLFA unit (DFF + AND + XOR) as a macro and standard cell. Synthesis & Place-and-Route: Show that a 32-bit SLFA can be placed & routed by standard EDA tools, in the regular, dense grid we detail. Benchmarking: Verify RTL code with formal methods. Synopsys VCS and UVM testbenches. Compare our SLFA's latency, power, and area against a traditional parallel-prefix adder of the same bit-width, synthesized in the same technology node. Verify our claims of logarithmic time delay and efficiency gains. Prove the core logic in a testable, physical form.	Define and verify basic blocks FPGA Prototype: Implement the SLFA as a Verilog/VHDL module with a focus on proving the finite state machine logic. Run FPGA tests, log data. Compare vs. traditional adders on power, area, maximum clock frequency, latency (cycles) and resource utilization.	Synthesizable RTL code for the CIM Adder UVM Tests Fully functional and verified arithmetic core Initial FPGA Timing/Power report A prototype proven 32-bit SLFA macro cell. Published results

Phase II: Integration to ASIC Design Standards | (Months 7-12)

Goals	Key Tasks	Deliverables
Build the full System on Chip datapath around the SLFA. Synthesizable RTL code for the Mining/AI ASIC architecture. High-Speed Emulation of ASIC architecture Verify with formal methods. Synopsys VCS and UVM testbenches Compare vs. traditional mining architectures	SHA-256 Datapath Design: The SLFA is the core of the ALU. We must design the complete SHA-256 hash engine, integrating the SLFA into the adder network required for the different functions. Control & Memory Hierarchy: Design the state machine that sequences the 64 rounds of SHA-256, manages message scheduling (Wt), etc. Multi-Core Tile Design: Create a single mining "core" that contains a complete SHA-256 engine. Then, tile hundreds or thousands of these cores onto a single die design. Power/performance analysis. Benchmark against SHA-256 mining workloads.	Mining efficiency metrics (Hashes/Joule) and noise/thermal measurements A complete, placed-and-routed design of a multi-core Bitcoin mining ASIC, ready for physical design. The biggest challenge lies in this phase: successfully integrating the elegant SLFA into a complete, high-frequency, power-dense SHA-256 system that can be tiled thousands of times on a chip. Timing/Power Report.

16-Month Timeline

Phase III: Integration to ASIC Manufacturing Standards | (Months 13-16)

Goals	Key Tasks	Deliverables
Synthesis and Net List for final tape-out ready SHA-256 Hashing Core/AI Accelerator. **Final Pre-Silicon Design**	ASIC Test Chip (Tape-Out): Move to a small-scale ASIC (e.g., 22nm or 28nm) containing a single SLFA block (e.g., 32-bit). The goal is not performance, but silicon validation—proving it works in real silicon, measuring actual power, timing, and area. Critical path optimization (Place & Route) Physical Circuit Board schematics. Assembly/testing PCB for Lab Validation with Oscilloscope/DAQ Prepare documentation demos and visualizations	A functional, high-hash-rate, high-efficiency Bitcoin Miner/AI Accelerator ready for full-chip tape-out. GDSII Tapeout-Ready Files Investor-Ready Benchmarks Manufacturer's Package (Benchmarks, Roadmap, Documentation, Files, etc.)

Follow-Up Actions: Integration to ASIC Manufacturing Standards

Board & System Design: Develop the miner hardware—PCB, power delivery, cooling (critical), and host controller.

Firmware & Software: Develop the low-level controller firmware and the host software for pool integration and management.

High-Volume Tape-Out: Partner with a foundry (TSMC, Samsung) to fabricate the full-scale mining ASIC in an optimal node.

Technology Readiness Level (TRL-3): From Math Theory, to Licensable IP, to SoC

Completed
(Founder Funded)

Phase 1
6 Months
$500K USD

Phases 2 & 3
10 Months
$6.1 Million USD

Hand-Over/Joint Development
Licensing Revenue

TRL	Definition	Exit Criteria
1	Basic principles observed and reported.	Peer reviewed publication of research underlying the proposed concept/application. **(Peer-reviewed Publications, International Conferences, etc).**
2	Technology concept and/or application formulated.	Documented description of the application/concept that addresses feasibility and benefit. **(Patent Application, Valuation, and Market Report).**
3	Analytical and experimental critical function and/or characteristic proof of concept.	Documented analytical/experimental results validating predictions of key parameters.
4	Component and/or breadboard validation in laboratory environment.	Documented test performance demonstrating agreement with analytical predictions. Documented definition of relevant environment.
5	Component and/or breadboard validation in relevant environment.	Documented test performance demonstrating agreement with analytical predictions. Documented definition of scaling requirements.
6	System/sub-system model or prototype demonstration in an operational environment.	Documented test performance demonstrating agreement with analytical predictions.
7	System prototype demonstration in an operational environment.	Documented test performance demonstrating agreement with analytical predictions.
8	Actual system completed and "flight qualified" through test and demonstration.	Documented test performance verifying analytical predictions.
9	Actual system flight proven through successful mission operations.	Documented operational results.

Team Structure

Overview

The success of our 16 month timeline to Pre Silicon files depends on the key hires of Senior Engineers, including a seasoned Tapeout Lead to own the physical mining design and ensure first-pass silicon success. This priority, key role, is for a Physical Design Engineer with enough experience to be Senior Staff Manager. We also require a dedicated development team working on the RTL to GDSII Flow, and a verification team dedicated to validating, testing, benchmarking, quality control and de-risking the design. Each team consists of one (1) Senior ASIC Engineer, two (2) Junior Engineers, and a support team of 1-2 graduate students. A third team of two engineers for Environment & Infrastructure Setup, Maintenance, and Support is also needed for operational support and to ensure the design engine runs smoothly. This team consists of one (1) Senior CAD Flow Engineer, and one (1) Script & Lab Building Engineer and is responsible for Setting up work workstations, Git Administration, and Lab Setup. Having dedicated teams for design and verification prevents conflicts of interest and ensures rigorous testing. This team structure covers Design→Verification→Tapeout while aligning with our adder's unique requirements. It is planned to be efficient, mitigate risk, avoid bottlenecks and enhance productivity in balance with the allocation of resources. Our team covers every critical function from high-level architecture to final sign-off.

Structure and Roles

Technical Execution Team

Senior ASIC Physical Design Engineer (Senior Staff Manager). A seasoned Tapeout Lead to own the physical design and ensure first-pass silicon success. This is the priority key role.

TEAM I: Dedicated development team working on the RTL to GDSII Flow to produce ASIC Net List and physical layout.

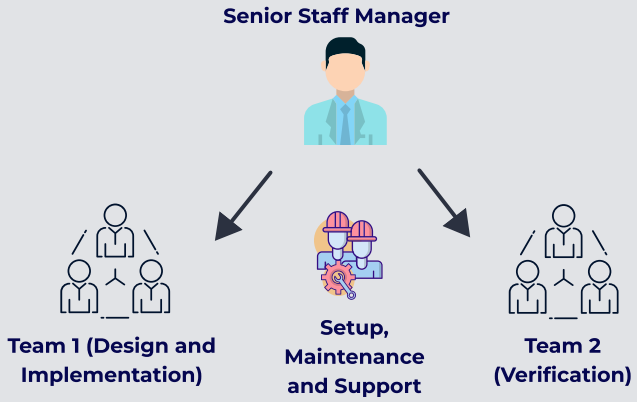
Senior ASIC Design Engs.

- RTL Integration Engineer
- Physical Implementation Engineer

TEAM II: A verification team to validate, test, benchmark, quality control and de-risk the design.

Senior FPGA Verification/Testing Engs.

- Test Development Engineer
- Power & Benchmarking Engineer



Team Structure

Structure and Roles

Environment & Infrastructure Setup, Maintenance, and Support

This team is operational support to ensure the design engine runs smoothly, and consists of one (1) Senior CAD Flow Engineer, and one (1) Script & Lab Building Engineer. Setting up work workstations, Git Administration, and Lab Setup.

- **Tooling and Infrastructure Setup:** Just setting up the version control (Git), continuous integration (CI) system, simulation environments, and FPGA toolchains for a new team can take a few weeks, and Tooling and environment problems are a major source of project delays.

- **Lab and Script Management:** Critical for toolflow, automation, and FPGA lab management. Operational Efficiency: The support roles are force multipliers that prevent our expensive engineers from getting bogged down in administrative or tooling issues. Tasks include Lab/Script building, managing, and support.

Graduate Students

Under our agreement, the University of Guadalajara will also allow lab hours, equipment and discounted licenses for Electronic Design Automation software and Physical Circuit Board machines. Graduate students assist with setup of environments, readiness, lab work, basic scripting, lab support and reports.

Administrative Management

Business Strategy, execution of administrative and legal matter tasks such as HR and contracts, IP matters, and finances freeing the technical team to focus on R&D.

Project Leadership

Juan Pablo Ramirez serves as Lead Architect, and Project General Manager. Knowledge sharing, System-level design and patented "Simple and Linear Fast Adder" Core for Compute-In-Memory Architecture.

Senior Staff Manager

Senior ASIC Physical Design Engineer

This key role is for a seasoned Senior Physical Design Engineer with experience in mining ASIC design, implementation and tapeout. He is the linchpin that transforms an RTL design into pre-silicon and constitutes the most crucial addition for tapeout success. We are seeking an experienced and highly motivated Senior ASIC Physical Design Manager to lead our Physical Design team. This critical role involves a blend of hands-on technical leadership, strategic planning, and people management. The successful candidate will be responsible for overseeing the complete physical implementation of complex Application-Specific Integrated Circuits (ASICs) and System-on-Chips (SoCs) from RTL to GDSII tapeout, ensuring all designs meet aggressive Power, Performance, and Area (PPA) targets. This manager will drive technical excellence, define implementation methodologies, and foster a culture of innovation and high performance within the team.

Key Responsibilities

- The manager will lead and manage the end-to-end physical implementation flow for complex ASIC/SoC designs, including block-level and top-level integration. This involves taking full ownership of the physical design from RTL to GDSII.

- A core responsibility is to drive and optimize the design for best-in-class Power, Performance, and Area (PPA) across all implementation stages, including floorplanning, power grid design, placement, Clock Tree Synthesis (CTS), routing, and final sign-off authority before GDSII is released. The role requires owning the timing closure process, which encompasses static timing analysis (STA), constraint generation and management.

- The manager will serve as the primary technical expert, providing guidance and hands-on support to resolve complex physical design challenges, such as congestion, timing violations, and power integrity issues. Makes high-stakes strategic decisions on timing closure, floorplanning, and power integrity.

- The manager must ensure successful sign-off for all critical checks, including physical verification (DRC/LVS), reliability (EM/IR-drop), and signal integrity. Defining, developing, and continuously improving the physical design methodology, flows, and tool scripts is essential to enhance the efficiency, predictability, and quality of all tapeouts.

- Tapeout preparation (7nm), including timing closure, power analysis, and Design Rule Checking/Layout Versus Schematic.

- Interfaces with the foundry.

Senior Staff Manager

Senior ASIC Physical Design Engineer

Management and Team Development

Leading, mentoring, and managing a team of physical design engineers is a key duty. Effective project management is required to plan, track, and manage project schedules, resources, and technical milestones, ensuring the on-time and high-quality delivery of physical design blocks and full chip tapeouts. The manager is responsible for performance management, including conducting performance reviews, setting clear goals, and managing the career development of team members. The role demands effective collaboration with cross-functional teams, including Architecture, RTL Design, Verification, and CAD/EDA, to align on design specifications, drive architectural feasibility studies, and ensure seamless integration. Finally, strong communication and presentation skills are necessary, with the ability to clearly articulate complex technical issues and solutions to both technical and executive audiences.

Required Qualifications

- **Education:** A Bachelor's or Master's degree in Electrical Engineering, Computer Engineering, or a closely related field is required.
- **Scripting and Automation:** Strong proficiency in scripting languages (e.g., TCL, Python, Perl) for flow automation and data analysis is required.
- **Tools:**
  - Vivado Design Suite
  - Cadence Design Suite
  - Synopsys Design Compiler (DC)
  - Siemens EDA
  - Innovus (Cadence) or ICC2 (Synopsys) for Place & Route
  - SPICE
  - RedHawk
  - PowerArtist

Nice-to-Have

- Experience with advanced packaging technologies (e.g., 2.5D, 3DIC) is highly desirable.
- Familiarity with front-end design and RTL methodologies is a plus.
- Experience with formal verification and equivalence checking tools is beneficial.
- Familiarity with Compute-In-Memory architectures.
- Relocation to Guadalajara, Mexico.

Must Have Skills

Experience: Experience: Candidates must have a minimum of 8+ years of experience in ASIC Physical Design, with at least 3+ years in a technical leadership or management role. and 2+ tapeouts:

- ASIC design flow (Synthesis, Place and Route, Static Timing Analysis).
- Has managed multiple tapeouts from start to finish.
- Tapeouts at ≤7nm (Bitcoin Mining ASICs).

- **Expertise in:**
  - Low-power RTL (Verilog/SystemVerilog)
  - RTL to GDSII flow
  - Technical Expertise: The candidate must possess deep, hands-on expertise in all aspects of the physical design flow (RTL-to-GDSII). This includes a proven track record of successfully leading multiple complex ASIC/SoC tapeouts in advanced process nodes (e.g., 7nm, 5nm, or below). Expert-level proficiency with industry-standard EDA tools from vendors like Synopsys (Fusion Compiler, ICC2, PrimeTime), Cadence (Innovus, Tempus), or Mentor Graphics is mandatory. Furthermore, a solid understanding of semiconductor physics, process technology effects on design, and low-power design techniques is essential.

- **Specialties:**
  - Clock Domain Crossing (CDC)
  - Static Timing Analysis (STA)
  - Power Integrity
  - Pipelining

Team 1

Senior ASIC Design Engineer (Team 1 Lead)

Expert in RTL design to Net List, synthesis, timing constraints, and low-power design. Understands the downstream physical effects of RTL decisions. Architect and review RTL for arithmetic core and ASIC. Manages medium to large size blocks.

Key Responsibilities

- Oversees Design Team
- Mentor Junior Engineers in Guadalajara via daily code reviews (GitLab) and weekly design/review sessions.
- Oversee RTL design, reviews, and development.
- Lead synthesis, timing closure, and physical design for mining ASIC.
- Develop and validate timing constraints (SDC) for the entire design.
- Generate Gate-Level Net List.
- Tapeout preparation including timing closure, power analysis, and Design Rule Checking/Layout Versus Schematic.
- Tapeout of ASIC Prototype.
- Front-end sign-off.

Nice-to-Have

- Familiarity with Compute-In-Memory architectures.
- Python/C++ for scripting and verification.
- Relocation to Guadalajara, Mexico

Must Have Skills

- **Experience:** 6+ years of experience in Bitcoin Mining ASIC design with 2+ tapeouts (in Bitcoin Mining or high-performance ASICs):
  - MACs (accumulators, matrix multipliers).
  - Memory interfaces (Phase Change Memory timing constraints).
  - ASIC design flow (Synthesis, Place and Route, Static Timing Analysis).
  - ASIC tapeout experience.
  - Tapeouts at ≤14nm (Bitcoin Mining ASICs).
- **Tools:**
  - SystemVerilog
  - DC/Genus (synthesis)
  - SDC (time constraints)
  - UPF (low-power design)
  - Vivado Design Suite
  - Cadence Design Suite
  - Synopsys Design Compiler (DC)
  - Verilog/VHDL
  - SPICE
  - PowerArtist
- **Expertise in:**
  - Low-power RTL (Verilog/SystemVerilog)
  - Universal Verification Methodology
  - RTL to GDSII flow
- **Specialties:**
  - Clock Domain Crossing (CDC)
  - Static Timing Analysis (STA)
  - Power Gating
  - Pipelining

Team 1

RTL Integration Engineer

RTL design Engineer. Familiarity with Static Timing Analysis for Mining ASIC. Code and verfify small to medium size blocks. Assists on large block creation.

Key Responsibilities

- Design and implementation in Verilog/VHDL.
- Ensures clean RTL coding.
- Develop and verify a dual-edge register that reads on rising edge and writes on falling edge (identify Phase Change Memory time constraints), on Verilog/VHDL.
- Implement Compute-In-Memory Adder RTL under lead architect's guidance.
- Develop and maintain automation scripts for the design flow (synthesis, linting).
- Execute synthesis trials and generate reports for the senior to analyze.
- Support synthesis, and design for testability.
- Collaborate with verification Engineers to validate designs.
- Mentor graduate students to maintain the design and integration documentation.

Nice-to-Have

- Experience with Bitcoin Mining ASICs (Hash-256).
- Familiarity with Compute-In-Memory Architectures
- Questa/NC-Sim
- Altera
- Quartus

Must Have Skills

- **Experience:** 3+ years in
  - RTL Design
  - ASIC Design Flow
    - Synthesis
    - Simulation
    - Place and Route
    - Static Timing Analysis
  - ASIC Verification
    - UVM
    - OVM
- **Tools:**
  - FPGA Prototyping and Toolchains
  - Verilog/SystemVerilog
  - Vivado Design Suite
  - VCS
  - Basic Python TcL for scripting
  - PowerArtist
  - SPICE
- **Expertise in:**
  - Memory Hierarchies (Cache, Registers)
  - Low-power RTL (Verilog/SystemVerilog)
  - Cadence Suite
  - Synopsys DC/VCS
  - Universal Verification Method
- **Specialties:**
  - Clock Edge Manipulation
  - Clock Domain Crossing (CDC)
  - Timing Analysis

Team 1

Physical Implementation Engineer

RTL design and verification Engineer. Familiarity with Static Timing Analysis for Mining ASIC.

Key Responsibilities

- Run place-and-route and physical verification tools under strict guidance from the Senior Staff lead.
- Violation Triage: Run DRC/LVS, categorize violations, and fix simple ones (e.g., spacing, shorted nets).
- Execute Engineering Change Orders (ECOs) for timing and functional fixes.
- Flow Support: Help maintain the physical design automation scripts.

Nice-to-Have

- Experience with Bitcoin Mining ASICs (Hash-256).
- Familiarity with Compute-In-Memory Architectures
- Questa/NC-Sim
- Altera
- Quartus

Must Have Skills

- **Experience:** 4+ years in
  - ASIC Design Flow
    - Place and Route
    - Static Timing Analysis
  - ASIC Verification
  - PCB Design (Schematics/Layout)
- **Tools:**
  - Innovus (Cadence Design Suite)
  - Vivado Design Suite
- **Expertise in:**
  - Memory Hierarchies (Cache, Registers)
  - Low-power RTL (Verilog/SystemVerilog)
  - Cadence Suite
  - DC/VCS (Synopsys)
- **Specialties:**
  - Clock Edge Manipulation
  - Clock Domain Crossing (CDC)
  - Timing Analysis

Team 2

Senior Verification Engineer (Team 2 Lead)

Testing is a Full-Time Parallel Effort. A separate verification team is best practice, and they must work in lockstep with the development team developing the test plan and testbenches, from day one. Writing tests as the RTL is being developed, running regression tests continuously, and debugging failures is a collaborative and time-consuming process that involves both teams. A single bug can take days or weeks to isolate and fix. An expert in SystemVerilog and the UVM methodology will lead this team.

Key Responsibilities

- Verification plan to define what needs to be tested and how to measure completeness.
- Write Universal Verification Methodology templates upfront to avoid verification delays.
- Synopsys DC-TCL scripts to automate synthesis checks.
- Testbench Architecture: Design the top-level UVM testbench for the entire SoC.
- Lead the effort to triage and root-cause simulation failures (Debugging).
- Prove verification closure through coverage metrics and Sign-Off.
- Mentor Junior Verification Engineers.

Nice-to-Have

- Familiarity with Compute-In-Memory architectures.
- ASIC tapeout experience.
- Python/C++ for scripting and verification.
- Relocation to Guadalajara, Mexico

Must Have Skills

- **Experience:** 6+ years in Bitcoin Mining ASIC design with 2+ tapeouts (in Bitcoin Mining or high-performance arithmetic):
  - Has built complex testbenches from the ground up.
  - Understands coverage-driven verification (code and functional coverage).
  - Memory interfaces (Phase Change Memory timing constraints).
- **Tools:**
  - AMD Alveo accelerator cards and Virtex 7 FPGA Kit
  - Vivado Design Suite
  - Synopsys Design Compiler (DC)
  - SPICE
  - Verdi (Synopsys)
- **Expertise in:**
  - Low-power RTL (Verilog/SystemVerilog)
  - Universal Verification Methodology
  - RTL to GDSII flow
- **Specialties:**
  - Clock Domain Crossing (CDC)
  - Static Timing Analysis (STA)
  - Power Gating
  - Pipelining

Team 2

Test Development Engineer

Validate adder performance and Compute-In-Memory compatibility. Emulating, and benchmarking the arithmetic core and the system-level ASIC implementation. This position requires a candidate with strong analytical and problem-solving skills.

Key Responsibilities

- Develop a wide range of directed and constrained-random tests.
- Write code to automatically verify the correctness of output data.
- Validation and Measurements.
- Emulate and Develop testbenches for dual-edge register.
- Emulate CIM Adder on Virtex 7 FPGA.
- Benchmark Proposed Adder vs. Traditional Adders.
- Benchmark ASIC Prototype with SHA-256 Workloads.
- Submit Recorded Lab Tests.
- Regress tests and collect coverage data.
- FPGA Prototyping Support and help port tests to the FPGA for hardware validation.

Must Have Skills

- **Experience:** 4+ years Hands-on experience with:
  - ASIC verification (UVM/OVM).
  - Data Analytics on Python/MATLAB.
  - FPGA Prototyping.
- **Tools:**
  - AMD Virtex 7 FPGA Kit and Alveo accelerator cards
  - Verilog/VHDL
  - VCS
  - Python
  - Grafana
- **Expertise in:**
  - Low-power RTL (Verilog/SystemVerilog).
  - Universal Verification Method.
- **Specialties:**
  - Ability to Troubleshoot Signal Integrity, Timing Closure
  - Clock Domain Crossing (CDC)
  - Timing Analysis

Nice-to-Have

- Experience with high-performance arithmetic ASICs (matrix multiplication).
- Siemens Veloce
- Cadence Palladium

Team 2

Power & Benchmarking Engineer

Verifying that the design is functionally correct is one thing. Proving it achieves the 30-40% performance/power improvement is another. This requires building complex testbenches with reference models, running extensive simulations with real-world mining workloads, and analyzing power and timing. This is a massive task in itself. Benchmarking Reports comparing our FPGA-emulated arithmetic core against traditional FPGA-implemented ALU cores. Key metrics include Maximum Clock Frequency (Speed), Resource Usage (LUTs, FFs, DSPs on the FPGA), Power Consumption Estimation (from the tools), and Latency (cycles to complete an operation).

Key Responsibilities

- Emulate CIM Adder on Virtex 7 FPGA.
- Create scripts to automate the collection and reporting of performance/power data.
- Develop tests to measure throughput, latency, and hashing performance.
- Work with the design team to run power estimation flows (vector-based and static) and generate power reports.
- Benchmark ASIC with SHA-256 Workloads.
- Submit Recorded Lab Tests.
- Design Test PCBs (KiCad) and Debug with Oscilloscopes/DAQ and Pre-Silicon Troubleshoot.
- Guarantees real-world performance.

Nice-to-Have

- Experience with high-performance mining ASICs.
- Siemens Veloce
- Cadence Palladium

Must Have Skills

- **Experience:** 4+ years Hands-on experience with:
  - Power/Performance Analysis (e.g., PrimePower).
  - ASIC verification (UVM/OVM).
  - Data Analytics on Python/MATLAB.
  - Lab skills (oscilloscopes, logic analyzers).
  - FPGA Prototyping and PCB Design.
  - Basic scripting skills (Python, Perl).
- **Tools:**
  - AMD Virtex 7 FPGA Kit and Alveo accelerator cards
  - PowerPro RTL Power Estimation (Siemens)
  - Verilog/VHDL
  - Lab equipment (oscilloscope, analyzers, etc.)
- **Expertise in:**
  - Low-power RTL (Verilog/SystemVerilog).
  - Universal Verification Method.
- **Specialties:**
  - Ability to Troubleshoot Signal Integrity, Timing Closure
  - Clock Domain Crossing (CDC)
  - Timing Analysis

Environment & Infrastructure Setup, Maintenance, and Support

Senior CAD Flow Engineer

Tooling and environment problems are a major source of project delays. freeing up the entire engineering team to design instead of dealing with tool issues. A Senior CAD engineer will handle the complex, high-value toolflow issues that can block our Engineers for days. We want a truly experienced individual who has worked at one of the major EDA companies (Synopsys, Cadence, Siemens) or a major semiconductor company. They don't just run scripts; they build and maintain the entire design automation flow, manage tool licenses, debug complex tool issues, and support the Physical Design Engineer. He ensures the design engine and tech stack runs smoothly.

Key Responsibilities

- Manage EDA tool licenses (Cadence, Synopsys, Siemens).
- Develop and maintain automated design flows (e.g., for RTL synthesis, place & route, simulation).
- Interface with EDA vendor support.
- Manage the PDK (Process Design Kit) from the foundry.
- Support the lab infrastructure (servers, workstations).
- Handles the complex, high-value toolflow issues that can block our Physical Design Engineer for days.

Must Have Skills

- **Experience:** 6+ years in CAD Flow development. Experience supporting a physical design team through multiple tapeouts.
  - CI/CD systems (GitLab CI/Jenkins)
  - Containerization (Docker)
- **Tools:** Expert-level proficiency in
  - Python
  - Tcl
  - Perl
  - Makefiles
  - Cadence & Synopsys tool suites and their automation interfaces.
- **Expertise in:**
  - Design Flow AutomationPDK Management
  - Compute Cluster Management
  - Continuous Integration
- **Specialties:**
  - Solving complex tool/flow issues
  - PDK customization
  - Resource optimization

Environment & Infrastructure Setup, Maintenance, and Support

Script & Lab Building Engineer

The Lab Manager handles the routine tasks, freeing up the entire engineering team to design instead of fighting tool issues. This person is more focused on the day-to-day operations. They manage the physical lab, FPGA boards, oscilloscopes, and logic analyzers. They handle server maintenance, software installations, and run routine scripts and regressions. We are looking for a very talented systems administrator with hardware affinity.

Key Responsibilities

- Maintain and congure FPGA development kits and lab equipment.
- Manage software installations and updates on workstations/servers.
- Handle data management and backup for the design team.
- Support the Senior CAD Flow Engineer.
- Lab Manager to handle routine tasks.

Must Have Skills

- **Experience:** 3+ years in
  - Lab Management or EDA support
  - Hands-on experience with hardware and software installation
- **Tools:**
  - Linux system administration
  - Bash/Python scripting
  - GitLab administration
  - VM/Docker management
  - Experience with server hardware and basic networking.
- **Expertise in:**
  - IT Infrastructure Support, Lab Equipment Management, Software License Management.
- **Specialties:**
  - Rapid troubleshooting
  - Automation of repetitive tasks

Graduate Students (1-2 on Each Team)

We will require assistance with critical but repetitive tasks to help free up engineers for core work. A team of three to four Graduate Students will be recruited to provide on-site support, stemming from our collaborative relationship with the University of Guadalajara (Mexico's second largest university located in the "Mexican Silicon Valley").

RTL Design (2)

- **Responsibilities**
  - Implement Dual-Edge Registers
  - Provide pre-configured Docker containers with EDA tools (avoid setup headaches).
  - Setup GitLab CI/CD to auto-run tests on RTL commits.
- **Tools:**
  - GitLab CI/CD for setting auto-run tests on RTL commits.
  - Verilog/VHDL
  - Yosys/Verilator
  - FPGA flow
  - Virtex-7 FPGA Kit
- **Experience:** 2+ years:
  - FPGA Prototyping.
  - UVM/OVM
  - Verilog contests (e.g., FPGA Olympics)
  - University tapeout projects.
  - PCB design competitions

Verification (1)

- **Responsibilities**
  - Develop UVM
  - Testbenches for Formal Verification.
  - Power/performance analysis on FPGA
  - Equipment Setup
  - Lab Support
  - Data Collection
    - Power Logs
    - Thermal Logs
- **Tools:**
  - KiCad
  - Oscilloscopes
  - Soldering
  - Python, Git, Linux
  - Virtex-7 FPGA Kit
- **Experience:** 2+ years hands-on:
  - Lab skills (oscilloscopes, logic analyzers).
  - UVM/OVM

Benchmarking (1)

- **Responsibilities**
  - Test Automation
  - Power/performance analysis on FPGA
  - Data Collection
    - Power Logs
    - Thermal Logs
  - Comparison Testbenches
- **Tools:**
  - GitLab CI/CD for setting auto-run tests on RTL commits.
  - Python scripts for automation
  - MATLAB
  - KiCad
  - Oscilloscopes
  - Python, Git, Linux
  - Virtex-7 FPGA Kit
- **Experience:** 2+ years hands-on:
  - Lab skills (oscilloscopes, logic analyzers).
  - UVM/OVM

Tools & Resources

Required Standards

Our selection of tools guarantees

- **Professional-Grade Verification:** Synopsys VCS and Cadence Xcelium ensures dual-edge registers and adder meet industry standards, and smoother future tapeouts.
- **Realistic Emulation:** High-Performance FPGA Kits such as Virtex 7 and Alveo accelerator cards support High-Bandwidth Memory for emulation of CIM Adder at scale, and benchmarking of mining-specific workloads (SHA-256 hashing) with realistic data.
- **Trusted Measurements:** Keysight oscilloscope provides reliable data for investors (e.g., "Our adder reduces latency by X%"). Validate dual-edge timing (200MHz+).
- **No Bottlenecks:** Engineers have dedicated high-end workstations.
- **Investor-Readyness:** Professional Tools = Credible Data.
- **Future Scalabillity:** Virtex and Alveo platforms support future ASIC development.

Workstations

Main Server: AMD EPYC 7302P equipped with Alveo U55C accelerator card. For running GitLab. Parallel CI/CD. Multiple FPGAs. RAID array for build backups.

Workstation I for Team 1: Ryzen 9 7950X equipped with Virtex 7 FPGA Kit. RTL Design. Basic emulation of small to medium size Blocks.

Workstation II for Team 2: Ryzen 9 7950X equipped with Virtex 7 FPGA Kit. Testing. Basic benchmarking.

Workstation III for Senior Physical Design Engineer: AMD Threadripper 7970X equipped with Alveo V80 accelerator card. RTL compilation. Real-time Emulation. Best FPGA performance. Mount Vivado projects from EPYC server to workstation using a Network File System. Supports TensorFlow for AI-assisted formal verification.

Remote Workstations for Senior Engineers (4): Lenovo ThinkPad P16 Gen 2. AMD Ryzen 9 PRO 7945HX. RTX 5000 ADA Generation. 128GB DDR5 ECC RAM. 10G Ethernet (server access). Requirements for remote connection to servers via X2GO.

Hardware

FPGAs
- AMD Virtex 7 (RTL Eng. WSI)
- AMD Virtex 7 (FPGA/Testing Eng. WSII)
- AMD Alveo V80 (ASIC Eng. WSIII)
- AMD Alveo U55C (Main Server)

Lab Instrumentation
- Oscilloscope
- Logical Analyzer
- Power Supply
- DAQ (Analog Data Acquisition)
- PCB Machine

Software

Open Source
- FABulous
- Icarus
- Grafana
- QEMU

Licensed
- Vivado
- Cadence
- Synopsys
- SPICE

Tools & Resources

Specifications

Workstations

Main Server

CPU: AMD EPYC 7302P (16C/32T, 3.3GHz). High core count for parallel CI/CD jobs.

Accelerator Card: Alveo U55C

Motherboard: ASUS KRPA-U16. 128x PCIe Gen3 lanes, IPMI for remote management.

RAM: 256GB (8x32GB) DDR4-3200 ECC RDIMM. Handles large emulation traces + multi-user loads.

Storage: 2x1TB Gen4 NVMe for primary. Plus 4x4TB SATA SSD (RAID10, GitLab storage, cache). Fast access for Vivado projects and artifact storage. Enterprise-level backup.

PSU: Dual Corsair 800W 80+ Platinum. 24/7 reliability for CI/CD uptime. Redundancy.

Networking: Dual 10G SFP+ (Mellanox ConnectX-4). High-speed GitLab runner communication.

RAID/HBA Card

Cooling: Passive heatsink. Noctua NH-U9 TR4-SP3. Specific for Ryzen Threadripper and Epyc processors.

Case: 4U Rackmount (Supermicro CSE-847). Fits 12x hot-swap drives + U55C accelerator card.

Workstation III

CPU: AMD Ryzen Threadripper 7970X (24C/48T). 5.3GHz boost accelerates RTL simulations (Vivado/Verilator).

Accelerator Card: Alveo V80 Large scale ASIC simulations.

GPU: NVIDIA RTX 5000 ADA Generation (32GB). Enterprise-grade ASIC verification, 24/7 reliability.

Motherboard: ASUS Pro WS TRX50-SAGE WIFI. 88x PCIe Gen4 lanes, ECC support, dual NICs.

RAM: 128GB (4x32GB) DDR5-5200 ECC. ECC prevents bit-flips during long emulations.

Storage: 2x2TB NVMe (Samsung 990). 14GB/s read/write for scratch files during Placing &Routing.

PSU: Corsair AX1600i (1600W 80+ Titanium). Handles Alveo V80's 250W + CPU/GPU spikes.

Cooling: Noctua NH-U14S TR4-SP3 + 6x 140mm fans. Keeps 7970X cool under sustained loads.

Case: Corsair 7000D Airflow. Fits Alveo V80 + airflow for 350W CPU.

Workstations I & II

CPU: Ryzen 9 7950X (16C/32T). Fast single-threaded performance for RTL sims/synthesis.

FPGA Kit: Virtex 7

GPU: RTX 4090 (24GB GDDR6X). Accelerated verification (VCS/Xcelium) and waveform debugging.

Motherboard: X670E. ASUS ROG, MSI, or Gigabyte.

RAM: 64GB DDR5-6000. Sufficient for block-level simulation (32-bit adders, FIFOs).

Storage: 2TB Gen4 NVMe. Fast access for Vivado projects.

PSU: Corsair RMx 850W 80+ Platinum.

Cooling: 360mm AIO or High-End Air (Noctua NH-D15).

Case: Lian Li, Fractal, or Corsair Mid-Tower.

Tools & Resources

Specifications

Hardware

Prerequisites. For collaboration: Notion (documenting decisions), Slack, Cadence Cloud (through University). Operating System: Linux (RHEL/CentOS) for EDA tools. Cloud Backup: AWS/GCP for design storage. Version Control: GitLab Enterprise or GitHubTeams.

FPGAs

AMD Virtex 7 (WS I and II) Virtex 7 FPGA VC709 Connectivity Kit comes with the VC709 Evaluation Board featuring XC7VX690T FPGA (690K LUTs, DDR3).	The VC709 Kit has enough resources (690K LUTs) for block-level emulation. The RTL and FPGA/Testing Engineer's workstations will be equipped with this Kit.
AMD Alveo V80 (WS III) Features Versal HBM XCV80 adaptive SoC device. Supports Vivado Design Suite.	Scalable and flexible high-level programmability. Parallel CI/CD. Multiple workloads. ASIC design, synthesis and compiling. This card will be hosted in the main server.
AMD Alveo U55C (Main Server) Alveo U55C accelerator card is built around the Virtex XCU55 UltraScale+ FPGA.	Emulate and benchmark CIM adder at scale, and mining-specific workloads (SHA-256 hashing) with realistic data. High-speed Emulation. Pre-silicon validation of full ASIC. Supports High-Bandwidth Memory. Hardware-Accelerated Verification. ASIC-style timing closure supported with Vivado Design Suite. The Senior ASIC Engineer's workstation will be equipped with this card.

Lab Instrumentation

Keysight InfiniiVision 3000X Oscilloscope	Debug high-speed signals (200MHz+). Keysight oscilloscope provides reliable data for investor pitches (e.g., "Our adder reduces latency by X%").
Saleae Logic Analyzer	Saleae Logic Analyzer
National Instruments DAQ	Data Acquisition System.
Physical Circuit Board Fabrication/Testing	KiCad-designed test boards.

Tools & Resources

Specifications

Software

Prerequisites

- Operating System: Linux (RHEL/CentOS) for EDA tools
- Collaboration: Notion (documenting decisions), Slack, Cadence Cloud
- Cloud Backup: AWS/GCP for design storage
- Version Control: GitLab Enterprise or GitHubTeam
- Containerized Toolchains: Docker
- Queue management for FPGA jobs: Redis

Open Source SW

FABulous

FABulous is an embedded FPGA framework designed to be portable across different process nodes. Supports customization and provides good area, power, and performance characteristics for the generated FPGA fabrics.

Integrates several open-source tools such as Yosys, ABC, VPR, and NextPNR. The framework includes templates for logic, arithmetic, memory, and I/O blocks, allowing users to stitch them or add fully customized blocks and primitives.

Yosys + NextPNR

Early custom register design RTL.

Synthesis. Place and Route.

Verilog/Icarus

To be used with the university's Cadence/Virtuoso.

Icarus is a Lightweight Verilog simulator.

GTKWave (RTL)

Waveform Visualization.

Debugging signals/timing of register design.

QEMU

Virtual Prototyping.

Emulate Custom hardware.

Grafana

Monitor Benchmarking.

An analytics and monitoring platform designed for every database, allowing users to visualize and understand their metrics through dynamic and reusable data-driven dashboards..

KiCad

PCB Design (for test boards).

Open-source alternative to Cadence.

Tools & Resources

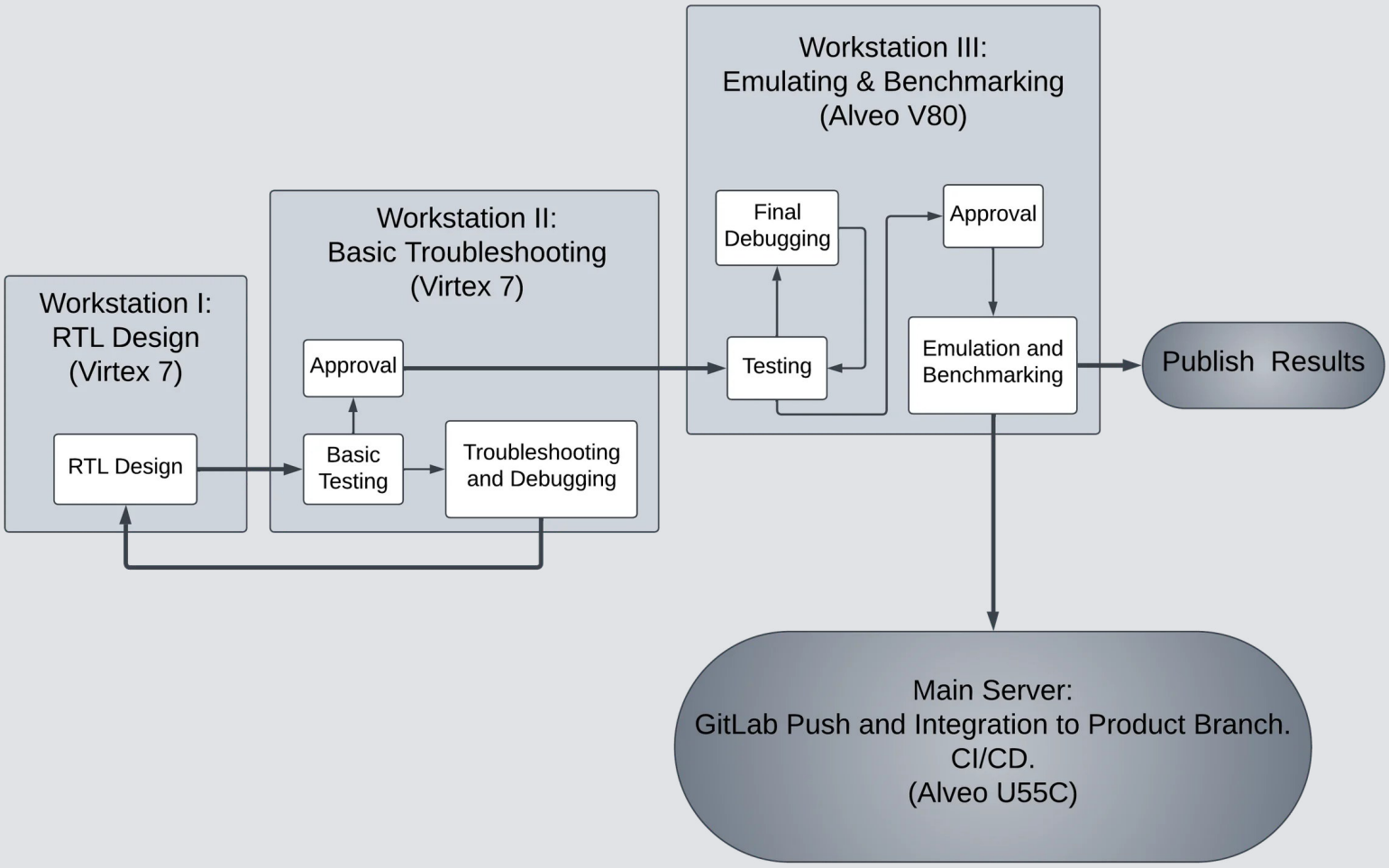
Specifications

Licensed EDA

Vivado Design Suite	Vitis: Synthesis/P&R. CLI automation.
Cadence Virtuoso	For custom register design. Implement adder and registers in Verilog using university's Cadence/Virtuoso.
Cadence Xcelium	Industry standard UVM verification.
Synopsys VCS	Mixed-signal simulation for dual-edge registers. VCS/Xcelium will ensure our dual-edge register and adder meet industry standards, making future tapeouts smoother.
Synopsys PrimeTime	For Static Timing Analysis to check for Dual-edge timing issues.
ModelSIM	Simulates behavioral RTL, and gate-level code delivering increased design quality and debug productivity with platform-independent compile. Single Kernel Simulator technology enables transparent mixing of VHDL and Verilog in one design. Advanced verification.
MATLAB + Simulink	Model analog effects with MATLAB/Python. Algorithm Modelling.
Cadence Genus	Synthesis.
Cadence Innovus	Physical design. Place and Route (P&R)
Ansys RedHawk	Power Benchmarking.
SPICE	Time Benchmarking.

Work Flow

Team Organization and Setup



Use of Funds

Our operational budget is of $6.6 Million USD to deliver a finished, tapeout-ready design to our manufacturing partners. Cash burn rate is of approximately $3.8 Million USD in the first year, and 1.7 Million USD in the second year. This funding will allow us to 1) Form and retain a world-class engineering team for 24 months to see this through from architecture to sign-off, 2) Procure the essential industry-grade software and hardware necessary to design and test to industry standards, and 3) Execute on our **16-Month Timeline**. With this investment, we will not be delivering just a paper concept or a partial prototype. **We will deliver a next generation processor in a final GDSII Stream File.** This asset is what we will license, and its value is confirmed by our third-party valuation for the underlying IP.

Concept	Resource
Team and Key Technical Hires (2 Year Salaries and Signing Bonuses)	**$3'750,000**
◦ **Senior ASIC Physical Design Engineer (Senior Staff Engineer)**	**$400k**
◦ **Senior ASIC Design Engineer**	**$300k**
◦ **Senior Verification Engineer**	**$300k**
◦ **Junior Engineers (4)**	**$800k**
▪ RTL to Pre-Silicon Design Engineers (2)	$400k
▪ FPGA/Verification Engineers (2)	$400k
◦ **Environment & Infrastructure Setup, Maintenance, and Support**	**$300k**
▪ Senior CAD Flow Engineer	$150k
▪ Script & Lab Building Engineer	$150k
◦ **Talent Accquisition: Signing and Relocation Bonuses, Recruiting Agency Fees**	**$1,000,000**
◦ **Core Team**	**$650k**
▪ Architect, Project Manager and CEO	$150k
▪ Fiscal, Legal and Internal Administration	$500k
Tools & Instruments	**$1,150,000**
◦ **Workstations**	**$65k**
▪ Main Server	$15k
▪ Team 1 Workstation (WS 1)	$10k
▪ Team 2 Workstation (WS 2)	$10k
▪ Sr. Staff Engineer Workstation (WS 3)	$10k
▪ Remote Workstations for Sr. Engineers (4)	$20k
◦ **Hardware**	**$85k**
▪ FPGA Kits	$50k
• Virtex 7 (2)	$20k
• Alveo U55C	$15k
• Alveo V80	$15k
▪ Lab Instrumentation	$35k
• Keysight InfiniiVision 3000X Oscilloscope	$5k
• Saleae Logic Analyzer	$5k
• DAQ system	$5k
• Physical Circuit Board Fabrication/Testing Equipment	$20k
◦ **Licensed EDA Software**	**$1,000,000**
▪ Vivado Design Suite	$100k
▪ Cadence Design Suite	$200k
▪ Synopsys Design Compiler and VCS	$400k
▪ Siemens Veloce	$150k
▪ Ansys RedHawk	$150k
Workspace for 15 persons in Guadalajara Metropolitan Area	**$250k**
▪ Two Years of Office Rent	$200k
▪ Basic Office Equipment	$50k
International Conferences, Publications	**$20k**
Marketing and Placement Agencies, Commercial Department	**$300k**
Collaboration with University of Guadalajara	**$30k**
◦ Graduate Students	
◦ Lab Hours, Workspace, and PCB Equipment	
Allocated Resources	**$5'500,000 USD**
Contingency Fund	**+20%**
TOTAL	**$6'600,000 USD**

THANK **YOU!**

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