IP RISK ANALYSIS

FOR THE IMPLEMENTATION OF:

A COMPUTE-IN-MEMORY ARITHMETIC CORE WITH
+85% EFFICIENCY AND THROUGHPUT GAINS
USING STANDARD CMOS TECHNOLOGY

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[ARRAY ARCHITECTURE, CORP.]

The SLFA project is technically validated, legally protected, and commercially compelling. The combination of a novel algorithmic foundation, proven RTL implementation, and a massive market actively seeking efficiency breakthroughs positions this technology for significant impact.

We have completed VHDL and SystemVerilog verification which is a critical milestone that de-risks the next stages of development. It proves the core innovation works. The remaining challenge is translating this architectural advantage into demonstrable silicon superiority. With focused execution, the SLFA could redefine the competitive landscape of Bitcoin mining, AI and other arithmetic intensive applications.

The technology works, now the primary challenge lies in quantifying its performance across different process nodes and ASIC types—an effort that will be pursued through FPGA emulation. While other CIM architectures similarly reduce data movement, they rely on experimental components or narrowly tailored designs; in contrast, this solution offers broader applicability, faster time-to-market, and lower R&D costs. Early licensing discussions are already feasible, though building and benchmarking a prototype would further enhance the IP's value and commercial readiness.

Index

"SLFA" International Patent Brief

1. SOLID PATENT STANDING

From an IP standpoint, the PCT application is advancing in eight major jurisdictions (US, China, Japan, Korea, India, Singapore, UK, and Canada), and has received a favorable written opinion from the USPTO with all claims approved.

- Filed via USPTO (ISA) with a favorable written opinion.

- All 15 claims passed without amendment — which is highly unusual and speaks to strong novelty, inventiveness, and industrial applicability. This means the entire core and scope of the invention is both valid and enforceable. It is also very rare for all claims to be accepted without amendment and speaks of a solid IP coverage.
  - **Novel:** The design is not disclosed in any prior art globally.
  - **Inventive:** The design is not an obvious variation of known circuits.
  - **Industrial Applicability:** Implemented with standard CMOS technology.

- National phase entered in key markets **(U.S., China, Japan, Korea, UK, Singapore, India, and Canada),** backed by IP firm Anuation, indicating professional prosecution and global strategy.

2. VALUATION

A third-party valuation from InTraCoM Group (Germany-based global patent valuation experts) places **current value at +$8 Million USD.** InTraCoM has extensive experience working with international blue-chip corporations, financial institutions, and technology-driven organizations, reinforcing the credibility and institutional rigor of this valuation. Additional market validation is provided through a third-party brokerage report (Patent Brokerage Report) from Anuation Research & Consulting LLP.

3. TECHNICAL FEASIBILITY

The patent describes a simple, linear adder implementable with existing transistor and memory tech. No exotic materials or experimental physics. Development Plan **ready for prototyping** using FPGA, and a standard path toward ASIC validation.

We have successfully **verified the SLFA algorithm through a Register-Transfer-Level simulation** in VHDL and System Verilog, proving its correctness, scalability, and synthesizability. This is a critical milestone. You can see our simulation code, results and EPWave examples for signal analysis online at EDA Playground. This simulation confirms:

- *Algorithmic Correctness:* The Finite State Machine operates as patented, **correctly performing addition with proper state transitions** and completion detection.
- *Scalability:* The architecture **scales "bit width" linearly** without fundamental changes, confirming the "linear growth and complexity" claimed in the patent.
- *Synthesizability:* The VHDL description is clean and **synthesizable, ready for the next stage** of development.

What This Simulation Represents

The simulations we have confirm the mathematical model and the finite state machine operation, and represents functional verification of the SLFA algorithm's logic and correctness. It confirms that **the finite state machine (FSM) operates as mathematically proven** in the patent, accurately performing addition across multiple test cases, including edge cases and random inputs. More specifically, this simulation demonstrates:

- *Algorithmic Correctness:* The SLFA executes addition in logarithmic time, with proper state transitions, carry handling, and completion detection.
- *Bit-Level Precision:* The XOR and AND operations are correctly applied in parallel, with the carry evolving through the FSM iterations.
- *Scalability:* The same architecture scales cleanly from 2-bit, to 4-bit, to 8-bit (or any bit width).

We have verified the behavior across thousands of test cycles, proving that the mathematical model translates faithfully to a synthesizable hardware description.

What This Simulation Does NOT Provide

This is not a physical silicon simulation. It does not reflect:

- *Power consumption:* There is no transistor-level modeling, switching activity data, or dynamic power estimation.
- *Real-time latency on silicon:* While the clock cycles are counted, the actual propagation delays, gate switching times, and physical wire delays are not modeled.
- *Compute-in-memory behavior:* The CIM nature of the SLFA, where memory and logic are integrated into a single regular grid, is not captured at this abstraction level. The simulation treats registers and logic as separate HDL constructs, not as physically co-located cells within a grid.

In short, this is a logic simulation, not a performance, power, or physical implementation benchmark. **Functional verification is the foundation upon which all subsequent design stages depend.** However, until we have silicon-proven performance data, any royalty above 1% is a hard sell for risk-averse semiconductor procurement teams. This is precisely why our pre-seed ask: $500k gets us the benchmark data that justifies premium pricing. With silicon demonstrated efficiency and performance results, we can deliver the hard data that matters: Tokens per dollar, Joules per Terahash, hashrate per dollar, etc. **The 3–5% ask becomes a data-backed negotiation,** not a speculative one.

RISK ANALYSIS

4. IP RISK

The SLFA is protected by WO2023220537A1 with family patents in multiple jurisdictions. The invention is based on a novel mathematical formulation, making it difficult to design around. The patent portfolio positions us well for both defensive protection and licensing.

- The IP asset is legally sound across all 15 claims.
  - Multiple claims cover variants of the design — pipeline versions, reduced power modes, different versions, etc.
  - If granted as-is in national phases, this will give wide protection from competitors trying to “design around” the core idea.
- Strong position if licensing, defending, or commercializing.

5. BUSINESS MODEL

Array's revenue model is value-priced, not cost-priced. In certain ASICs our adder arrays dominate the silicon footprint and define the efficiency curve. This is not a commodity IP license; it is a bottleneck-defining architecture with zero substitutes and a mathematically-founded patent moat.

- *Fabless Licensing Model:* We operate under a **highly scalable, high-margin Fabless IP Licensing Model** (analogous to ARM or Rambus), avoiding all physical packaging, foundry allocation, macro supply chain, and retail logistics risks.
- *Different Verticals:* License our arithmetic cores to manufacturers across distinct computing fields (AI, HPC, Cryptography, Edge, and DSP) to maximize revenue capture across the $500B+ semiconductor ecosystem. In the Bitcoin mining ASIC vertical, our core cuts out on-chip data transfer to drive an **estimated 75% to 100% increase in mining bottom-line profitability. In the AI & LLM industry, we expect to deliver up to 85% energy efficiency and time performance gains over traditional hardware.** Manufacturers and design houses are locked in an efficiency race. Licensing the SLFA could give one of them a decisive competitive advantage, so we will offer non-exclusive licenses.
- *Revenue Streams:* Our streams are anchored on clear, high-conviction value capture: **upfront licensing fees,** continuous running royalties **(1–5% of gross chip sales),** or digital asset yields **(3–5% of mined tokens).**

6. MARKET CONTEXT

The Bitcoin mining ASIC market is intensely focused on Joules per Terahash (J/TH), the metric that determines profitability. Current-generation machines operate at 15–20 J/TH., with aggressively pushing toward sub-10 J/TH. **The SLFA's Compute-in-Memory architecture directly addresses the primary energy cost in current ASICs:** data movement between registers and logic. By eliminating this bottleneck, the SLFA will outperform existing parallel adders and increase energy efficiency. The market is actively seeking exactly this kind of breakthrough.

RECCOMMENDED ACTION

Since the ISA outcome is this positive, you're in a strong position to:

- Secure an agreement with robust IP clauses (e.g., licensing scope, royalty floor, profit-sharing from ASIC sales/mining).
- Request a copy of the ISR and WO/ISA Written Opinion for your records and due binder.
- Verify national phase entries (should match filing data in U.S., China, Japan, etc.)—all reflect the same unamended claims.
- Strong position if licensing, defending, or commercializing.

SUMMARY

This is a technically sound, legally strong, and implementation-ready IP asset — with a favorable international search report from the USPTO and zero required amendments. Low-IP-risk, Low-tech-risk, high-upside opportunity.

- Strong IP
- Practical tech
- Global patent coverage
- Defined ROI model
- A motivated team with real progress made

Final Assessment

CATEGORY	
Patent Quality	High — 15 unamended claims approved by USPTO-ISA, national phase entered in key jurisdictions, managed by professional IP firm (Anuation).
Technical Risk	Moderate to Low — FPGA emulation planned, design based on standard logic and compatible with existing semiconductor processes.
Implementation Readiness	Solid — Roadmap in place, no exotic materials or speculative components, investor handles mining ops.
IP Risk	Very Low — Favorable international search opinion, broad scope, legally defensible.
Market Strategy	Clear — Patent monetization through licensing and direct application in mining ASICs
Investor Leverage	High — Investment secures rights and a 20% stake in revenue-generating operations.
Third-Party Valuation	Intracom (Germany) values IP at $8M — supports credibility and future exit potential.

This is a low-IP-risk, low-tech-risk, high-upside opportunity with well-structured patent coverage, and a clear path to implementation. Assuming milestones are met (FPGA emulation, roadmap compliance, licensing terms), this proposal is strategically aligned for investment.

Q & A

"If this is so simple, why hasn't anyone done it before?"
For decades the industry has optimized the carry-propagation algorithm, not replaced it. This takes a mathematician redefining addition from first principles because it is a domain outside conventional digital design. Although easy to understand, the solution is counterintuitive to engineers trained in the carry-chain paradigm.

"Is this analog? What about noise and process variation?"
Fully digital. Standard CMOS logic. No interpreting analog current levels or probabilistic error correction. It behaves exactly like any standard digital block in any CMOS library. No exotic design, principles, materials or components.

"Can't a big player just copy this?"
While the Two-Input Adder is a valuable asset, the real value and industrial applicability comes from scaling into a Multiple-Input Adder. This is not a trivial jump, but we have matured the underlying designs in-house, giving us a long head-start. Furthermore, we do not seek to compete, rather license our IP arithmetic cores to design houses and manufacturers. That is a stronger moat than a circuit patent. Additionally, the architecture is non-obvious to engineers entrenched in traditional adder design. More than half a century of carry-propagate thinking is our best defence.

"What stops them from designing around it?"
The algorithm is the addition operation. To add two numbers without our design, you must revert to some form of Carry-Propagation paradigm of addition. There is no third way. We have protected the only alternative.

"Where's the silicon?"
We have peer-reviewed and published RTL and logic synthesis which is the first step in taking any prototype to Silicon. The Pre-Seed round is to verify and benchmark an emulated arithmetic core — moving from validated IP to proven performance data. The Seed round is for integrating the arithmetic core into a fully functional System-on-Chip Bitcoin Mining Engine or AI Accelerator. Probability of success is therefore not a matter of 'if it works, but of 'how well it performs' in a given process node and ASIC type.

"What's the real power/performance advantage? Give me a number."
For a 32-bit addition: logarithmic average iterations (≈5), constant gate depth per iteration, and zero data-movement energy. That eliminates most of the energy cost attributed to memory-to-ALU data transfer which is the main driver in power consumption and time.latency. We will deliver exact normalized metrics (energy per addition, throughput) from the pre-seed prototype, to verify +85% increase in efficiency and performance.

THANK **YOU!**

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