IP RISK ANALYSIS

FOR THE IMPLEMENTATION OF:

A COMPUTE-IN-MEMORY ARITHMETIC CORE WITH
+85% EFFICIENCY AND THROUGHPUT GAINS
USING STANDARD CMOS TECHNOLOGY

www.fastarithmeticunits-dataroom.com

[ARRAY ARCHITECTURE, CORP.]

Addition is a deterministic algorithm, and **our Simple and Linear Fast Adder is an easy to understand and analyze circuit** that executes a proven mathematical theorem. It is not a complex design with unpredictable behavior. Peer-reviewed proofs of its functional correctness and time-to-stability have been published. Aside from the theoretical foundations and mathematical algorithms published, the circuit logic, and RTL design have been detailed in numerous international conferences and peer-reviewed publications. **The proposed Compute-In-Memory (CIM) adder architecture is not contingent on new component technology or manufacturing processes.** It is completely achievable using standard CMOS transistors and memory cells, and is **generalized in rectangular arrays that can execute general operations such as matrix multiplication (for AI, and graphics processing) and the 64-round compression funciton of the SHA-256 (BC Mining), among others.**

An international PCT patent application is currently in national phase in eight key jurisdictions: US, China, Japan, Korea, India, Singapore, UK, and Canada. **The patent has received a favorable written opinion from the International Searching Authority (USPTO) with all 15 claims approved without amendment**—a rare outcome indicating strong novelty and industrial applicability. **A third-party valuation from InTraCoM Group (Germany-based global patent valuation experts) places current value at +$8 Million USD.** InTraCoM has extensive experience working with international blue-chip corporations, financial institutions, and technology-driven organizations, reinforcing the credibility and institutional rigor of this valuation. Additionally, we have a **comprehensive technology and market report (Patent Brokerage Report) from Anuation Research & Consulting LLP,** including a detailed market study that illustrates the practical usability of the product and demonstrates real-world applications of the underlying technology, which can be shared to support further evaluation and commercial understanding.

Probability of success is therefore not a matter of 'if it works, but of 'how well it performs' in a given process node and ASIC type. That performance is what we will benchmark via FPGA emulation of the RTL design. **We can infer and project performance and efficiency gains, based on other Compute-In-Memory architectures that cut out similar data movement,** although they cut out data movement through other means (experimental transistor types; segmenting subunits and relocating them; super-specific ASIC designs).

The main differences between our CIM arithmetic core and other CIM schemes are the time-to-market, universality of applicability, and R+D costs. We are positioned to initiate early-stage licensing discussions, while recognizing that building and benchmarking a prototype will significantly enhance both the value and commercial readiness of the IP.

Index

Q & A

"If this is so simple, why hasn't anyone done it before?"
For decades the industry has optimized the carry-propagation algorithm, not replaced it. This takes a mathematician redefining addition from first principles because it is a domain outside conventional digital design. Although easy to understand, the solution is counterintuitive to engineers trained in the carry-chain paradigm.

"Is this analog? What about noise and process variation?"
Fully digital. Standard CMOS logic. No interpreting analog current levels or probabilistic error correction. It behaves exactly like any standard digital block in any CMOS library. No exotic design, principles, materials or components.

"Can't a big player just copy this?"
While the Two-Input Adder is a valuable asset, the real value and industrial applicability comes from scaling into a Multiple-Input Adder. This is not a trivial jump, but we have matured the underlying designs in-house, giving us a long head-start. Furthermore, we do not seek to compete, rather license our IP arithmetic cores to design houses and manufacturers. That is a stronger moat than a circuit patent. Additionally, the architecture is non-obvious to engineers entrenched in traditional adder design. More than half a century of carry-propagate thinking is our best defence.

"What stops them from designing around it?"
The algorithm is the addition operation. To add two numbers without our design, you must revert to some form of Carry-Propagation paradigm of addition. There is no third way. We have protected the only alternative.

"Where's the silicon?"
We have peer-reviewed and published RTL and logic synthesis which is the first step in taking any prototype to Silicon. The Pre-Seed round is to verify and benchmark an emulated arithmetic core — moving from validated IP to proven performance data. The Seed round is for integrating the arithmetic core into a fully functional System-on-Chip Bitcoin Mining Engine or AI Accelerator. Probability of success is therefore not a matter of 'if it works, but of 'how well it performs' in a given process node and ASIC type.

"What's the real power/performance advantage? Give me a number."
For a 32-bit addition: logarithmic average iterations (≈5), constant gate depth per iteration, and zero data-movement energy. That eliminates most of the energy cost attributed to memory-to-ALU data transfer whcih is the main driver in power consumption and time.latency. We will deliver exact normalized metrics (energy per addition, throughput) from the pre-seed prototype, to verify +85% increase in efficiency and performance.

"SLFA" International Patent Brief

1. SOLID PATENT STANDING

- Filed via USPTO (ISA) with a favorable written opinion.
- All 15 claims passed without amendment — which is highly unusual and speaks to strong novelty, inventiveness, and industrial applicability. This means the entire core and scope of the invention is both valid and enforceable. It is also very rare for all claims to be accepted without amendment and speaks of a solid IP coverage.
  - **Novel:** The design is not disclosed in any prior art globally.
  - **Inventive:** The design is not an obvious variation of known circuits.
  - **Industrial Applicability:** It can be implemented with current technology (FPGAs/ASICs).
- National phase entered in all key markets **(U.S., China, Japan, Korea, UK, Singapore, India, and Canada),** backed by the Indian IP firm Anuation — indicating professional prosecution and global strategy.

2. TECHNICAL FEASIBILITY

The next two years are about further **de-risking the technology at a physical level and creating the licensable asset** (GDSII tape-out ready Stream File), with a **Pre-Seed investment of $6.6 MIllion USD.** Our cash burn-rate will be primarily driven by the engineering team's salaries, signing bonuses, tools, and resources. This investment is divided into two stages.

- Patent describes a simple, linear adder implementable with existing transistor and memory tech — no exotic materials or experimental physics.
- Development Plan ready for prototyping using FPGA, and a standard path toward ASIC validation.
- The implementation can be integrated into mining ASICs in the form of a Compute-In-Memory HASH Engine.

3. VALUATION AND MARKET STRATEGY

- Third-party valuation from Intracom (Germany) places the **patent's current value at $8 Million USD,** passing through experts who have vetted the invention. The value will increase during 2026, as the selected jurisdictions approve the application (national phase entered in May 2025), and we move to prototype.
- We´re offering a lifetime stake in a mining operation that will use the ASICs we design, acquired from licensing our design to existing ASIC manufacturers.

RISK ANALYSIS

1. IP RISK

- You’re not betting on uncertain patentability.
- The IP asset is already legally sound across all 15 claims.
- Strong position if licensing, defending, or commercializing.

2. BROAD AND DEFENSIBLE COVERAGE

- Multiple claims cover variants of the design — pipeline versions, reduced power modes, different versions, etc.
- If granted as-is in national phases, this will give wide protection from competitors trying to “design around” the core idea.

3. FASTER TIME TO GRANT

- You’re not betting on uncertain patentability.
- The IP asset is already legally sound across all 15 claims.
- Strong position if licensing, defending, or commercializing.

RECCOMENDED ACTION

Since the ISA outcome is this positive, you're in a strong position to:

- Secure an agreement with robust IP clauses (e.g., licensing scope, royalty floor, profit-sharing from ASIC sales/mining).
- Request a copy of the ISR and WO/ISA Written Opinion for your records and due binder.
- Verify national phase entries (should match filing data in U.S., China, Japan, etc.)—all reflect the same unamended claims.
- Strong position if licensing, defending, or commercializing.

SUMMARY

This is a technically sound, legally strong, and implementation-ready IP asset — with a favorable international search report from the USPTO and zero required amendments. Low-IP-risk, Low-tech-risk, high-upside opportunity.

- Strong IP
- Practical tech
- Global patent coverage
- Defined ROI model
- A motivated team with real progress made

Final Assessment

CATEGORY	
Patent Quality	High — 15 unamended claims approved by USPTO-ISA, national phase entered in key jurisdictions, managed by professional IP firm (Anuation).
Technical Risk	Moderate to Low — FPGA emulation planned, design based on standard logic and compatible with existing semiconductor processes.
Implementation Readiness	Solid — Roadmap in place, no exotic materials or speculative components, investor handles mining ops.
IP Risk	Very Low — Favorable international search opinion, broad scope, legally defensible.
Market Strategy	Clear — Patent monetization through licensing and direct application in mining ASICs
Investor Leverage	High — Investment secures rights and a 20% stake in revenue-generating operations.
Third-Party Valuation	Intracom (Germany) values IP at $8M — supports credibility and future exit potential.

This is a low-IP-risk, low-tech-risk, high-upside opportunity with well-structured patent coverage, and a clear path to implementation. Assuming milestones are met (FPGA emulation, roadmap compliance, licensing terms), this proposal is strategically aligned for investment.

Juan Pablo Ramirez
Architect, Project Manager & CEO
jramirez@binaryprojx.com

Pablo César Vázquez Estrella
Chief Financial Officer
pablo.vazquez@binaryprojx.com

Sergio Adrián Trujillo González
Senior Software Engineer
sergio.trujillo@binaryprojx.com

Héctor Alejandro Galvez López
Consultant in Elec. Eng.
University of Guadalajara
hgalvez@binaryprojx.com

THANK YOU!

www.fastarithmeticunits-dataroom.com

[ARRAY ARCHITECTURE, CORP.]